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HIGH INTEGRATED CIRCUIT

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[There are no amendments to this patent.]

Abstract (amended)

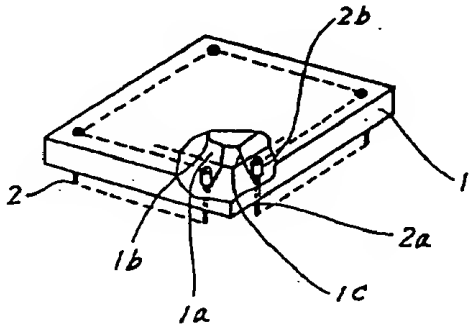
Objective

To realize a suitable LSI packing method for suppressing the influence of a timing display being a problem in the high-speed

operation of a logic circuit, particularly in an information processing device.

Constitution

In LSIs, signal pins are installed at the lower part, with connecting sockets of the same signal being installed at the upper part. A common bus signal such as that of a CPU bus and system bus is distributed to LSI signals; said several LSIs are stacked and packed, or the common bus signal is constituted by said several LSIs, packed in accordance with the pin arrangement of the LSIs having said common bus signal, and packed on said LSIs, so that a high-speed signal is connected at the shortest distance.



Claims

1. A highly integrated circuit characterized by the fact that in said highly integrated circuit (LSI) in which ICs, diodes, etc., are packed on a wafer and sealed with a mold or

ceramic, signal connecting pins are arranged at the lower part, and characterized in that pin sockets for connecting the same signal are arranged at the upper part.

2. A packing method characterized by the fact that signal lines are connected at the shortest distance by stacking several of the highly integrated circuits of Claim 1.

3. A packing method characterized by the fact that in the packing method of Claim 2, several integrated circuits are arranged to fit the pin arrangement of said highly integrated circuits, and in that the highly integrated circuits are packed on them.

4. An information processing device characterized by the fact that, using the highly integrated circuits of Claim 3, connecting pins are constituted by control signals of a system bus and I/F signals of a device, and in that the I/F signals of the device, are in connected by a cable, etc., from the stacked highly integrated circuits.

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